One extra resistor fights IC op-amp oscillations

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IC op amps don't like capacitive loads. They protest by oscillating. Classic ways of dealing with the problem usually result in unacceptably high closed-loop output impedance. Here's a simple way to obtain output impedance that stays low at frequencies out to the megahertz region.

Driving capacitive loads with IC op amps has caused trouble since Fairchild Semiconductor introduced the μA709 op amp in the mid-1960s. With a capacitive load, the circuit tends to be unstable to the point of oscillation. Because of this problem, much has been written over the years about driving capacitive loads. The following design concepts, some of which have never before appeared in print, shed some new light on the subject.

As a general rule, designers try to avoid capacitive loads. But if an op-amp circuit must have low output impedance over a wide frequency range, load capacitance usually becomes necessary. IC manufacturers' recommended circuit for isolating a capacitive load from an op-amp feedback loop yields a peak output impedance that is too high for many applications. However, you can add one resistor to the recommended circuit and reduce the output impedance by more than an order of magnitude. You can also see that the performance of real circuits compares with the results of Spice simulations. Two of the circuits use Analog Devices' (Norwood, MA) AD706J. One circuit has an output impedance that typically does not exceed 10Ω; the other maintains a constant 10Ω. A third circuit, which has a maximum output impedance of 250 mΩ, uses the SGS Thomson (Lincoln, MA) L2726 power op amp.

In 1992, I was challenged to design a buffer amplifier that could sink 200 mA and maintain a broadband output impedance of less than 1Ω. None of the usual techniques that use low-impedance buffers worked, so I set out to find a better option. The main problem was to reduce the output impedance. Finding an op amp that already had a low output resistance would simplify the task. The SGS L2726 power op amp has an output resistance of less than 4Ω when it sinks 10 mA or more. That was a good start.

To reduce the impedance even more, I tried to figure out how to get the isolation resistor—the one between the op-amp output and the capacitive load—inside a feedback loop. Output resistance inside a feedback loop is divided by loop gain. After three days of looking at many approaches, I discovered that by tapping just a fraction of the signal across this isolation resistor, I could achieve the necessary freedom from oscillation. After discovering that the circuit worked, I spent many days on Spice simulations to figure out why. Since discovering the circuit in 1992, I've found that the number of applications seems unlimited. All of the circuits discussed are voltage followers, but other configurations, such as inverting amplifiers, work equally well.

Today, some manufacturers offer precision op amps that have greatly improved capacitive-load-drive capabilities. Analog Devices' AD704/5/6 series and Linear Technology's (Milpitas, CA) LT1112 series are two examples. Although these units have excessive output ringing with step input voltages, the circuits don't oscillate with capacitive loads of 10 nF or more. Even so, output impedance is too high for many applications.

Many applications

Applications that can benefit from the new circuit include programmable voltage references for high-speed comparators, termination-resistor voltage references, DAC "reference-stick" center-balance drivers, IC-current-source base-voltage references, and programmable power sources. These circuits need not have high-frequency throughput, but they must have a minimal output-voltage deviation when subjected to load-current changes over a wide frequency range.

Analog Devices' home page, www.analog.com, was the

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source of the AD706J worst-case Spice model, which these simulations use. I could not find Spice models for SGS' L2726, so I made measurements on a device and created a simple model. I made the first measurement on the AD706J Spice model to see what the amplifier's output impedance looks like in a voltage-follower configuration (**Figure 1a**). I injected a 1-mA current into the output over the frequency range of 1 Hz to 100 MHz.

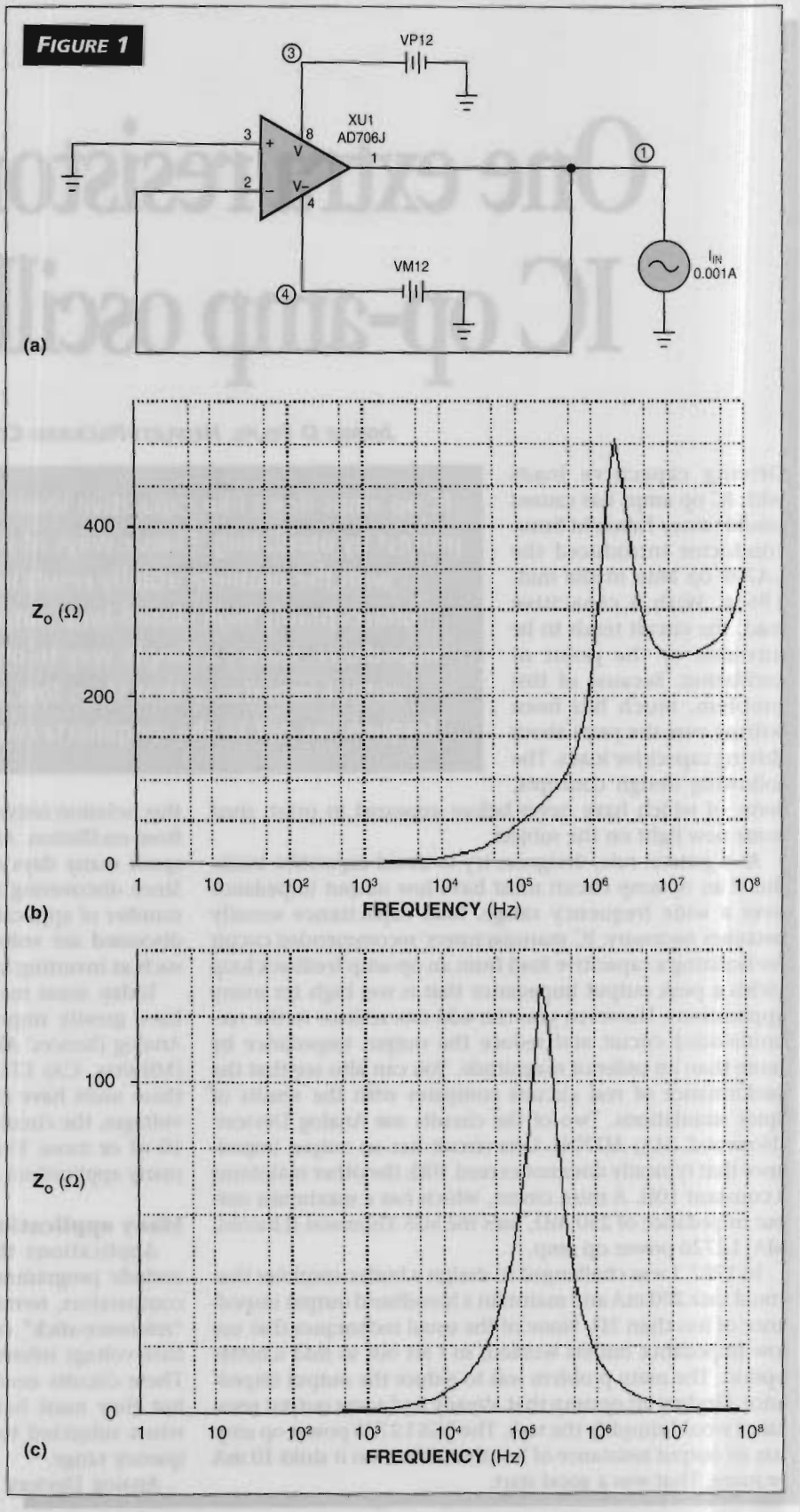
In **Figure 1b**, notice that the impedance reaches a peak of 500Ω (500 mV/1 mA) at approximately 2 MHz. When you add a 10-nF load capacitor, the output impedance improves to a peak of 130Ω at approximately 200 kHz (**Figure 1c**). **Figure 2a** is the circuit that most IC manufacturers recommend for driving large capacitive loads (in this case, 1 μF). The peak output impedance approximately equals the capacitive-load-isolation resistor, R_1 (**Figure 2b**).

A good rule of thumb is to choose R_1 to be approximately equal to the open-loop output resistance. The 1992 AD705J data sheet shows the op-amp's open-loop output resistance, R_O, to be typically 200Ω. (The AD705J is just a single version of the AD706J dual op-amp.) An inner feedback loop formed by C_2 and R_2 takes over the main outer feedback loop at a frequency equal to or less than the pole formed by R_1 and C_1. That is, $f=1/(2\pi R_1 C_1)=796$ Hz. The section "Lowering Z_O by a factor of 20" provides details of the loop design.

Data sheets don't specify R_O

You must know the op amp's open-loop frequency response, A_{OL}, and R_O before you can design these circuits. Normally, the data sheet includes a

FIGURE 1



To determine the device's output impedance as a function of frequency, the author injected a swept-frequency 1-mA current into the output of an AD706 Spice model (a) connected as a unity-gain follower. The AD706 voltage follower exhibits a closed-loop output impedance, Z_O, that peaks at approximately 500Ω at about 2 MHz (b). With the capacitive load, the output impedance peaks at approximately 130Ω at 200 kHz (c).

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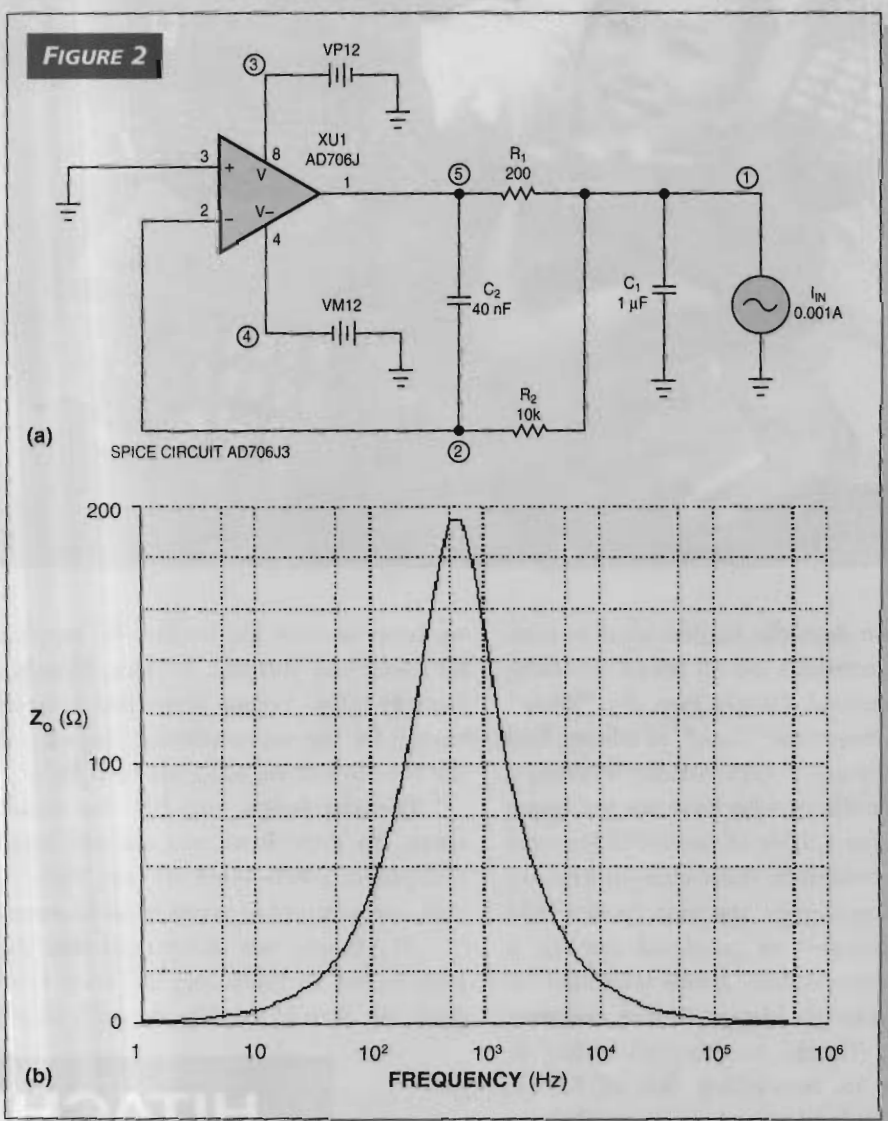
Bode plot of the typical open-loop frequency response but not of the open-loop output resistance. You can measure an op amp's open-loop frequency response in a closed-loop configuration by inserting a floating excitation source, V_{EX}, in series with the loop (**Figure 3a**.) This technique works as well on hardware as it does in Spice simulations. A small resistor, R_1, loads the excitation source. R_1 is unnecessary for Spice simulations, but it represents what the circuit looks like when you make measurements on hardware. R_1 also lets you comment V_{EX} out of the simulation. Adding this source must not alter the loop performance. That means that you must drive the source from a low impedance and load it with a high impedance. You may have to add buffers to the loop, and they, too, must not alter the loop performance.

This Spice simulation meets the impedance requirements by driving the excitation source from a low source impedance, E_1, and loading the source with a high impedance, XU1 Pin 2. The input to the loop is Node 2; the output is Node 5. You can use this technique to measure the response of any portion of the loop. **Figure 3b** shows the open-loop gain response. Compare this worst-case response with the typical response shown in the AD706J data sheet. An op amp's closed-loop output resistance is the open-loop output resistance divided by the loop gain (for loop gains above unity). Therefore, you can measure the open-loop output resistance in a closed loop as long as you make the measurement at frequencies at which the loop gain is less than 1.

The circuit in **Figure 4a** has a closed-loop gain of 60 dB. The op-amp runs out of loop gain above 500 Hz, where the 60-dB loop gain intersects the open-loop response. The closed-loop output impedance of this circuit is low at low frequencies but rises to the open-loop value at higher frequencies, where there is no more loop gain available to reduce the impedance. The simulation in **Figure 4b** exhibits an open-loop output resistance of 250Ω. If you measure this resistance on hardware, you will probably need to insert a capacitor between R_2 and ground to reduce the amplifier's output-offset voltage.

FIGURE 2



Op-amp manufacturers usually recommend that you stabilize a voltage follower by adding isolation resistor R_1 between the IC output and the circuit output (a). You then provide dc feedback from the circuit output via R_2 and ac feedback from the op-amp output via C_2. With classic stabilization, the peak output impedance is about equal to the value of the stabilization resistor you place in series with the op-amp output (b).

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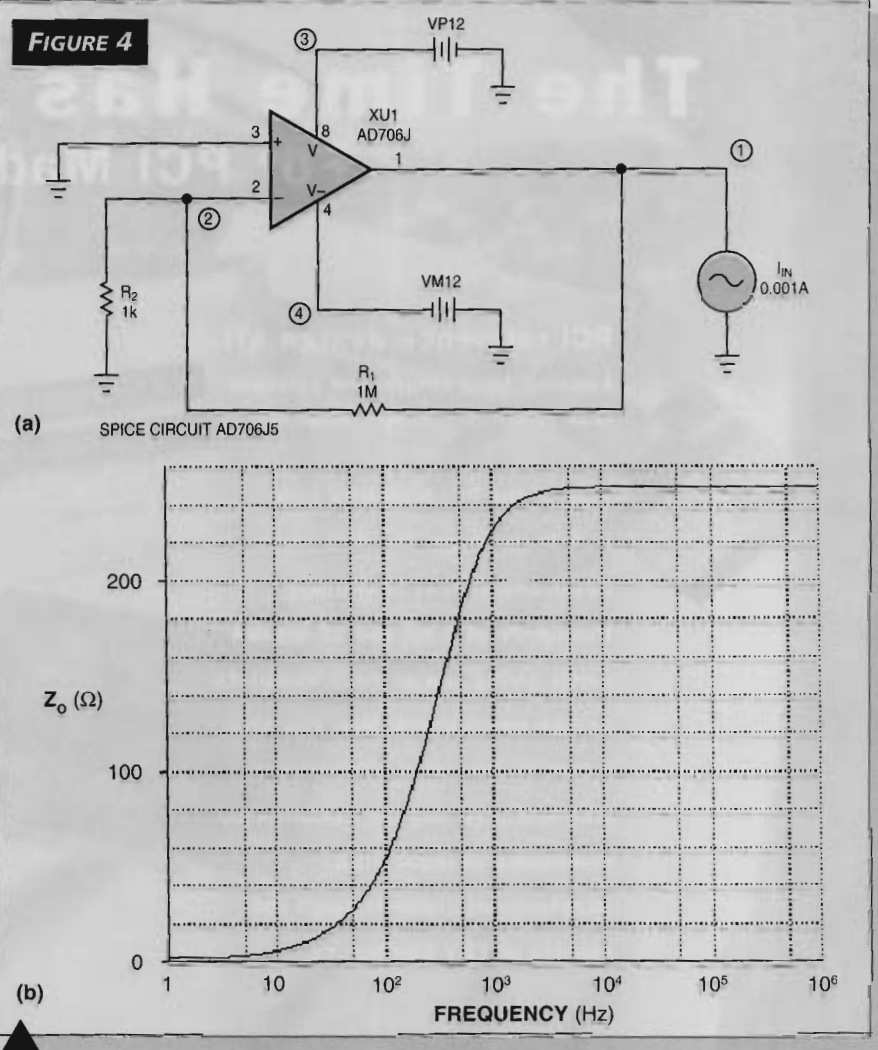
Now, if you go back to **Figure 2a** and insert an excitation source, V_{EX} (**Figures 3a** and **5a**), you can examine the effects of the capacitive-load circuit on the open-loop-gain response. **Figure 5b** shows the AD706J response in the upper curve (with no capacitive load) and the response of **Figure 5a** in the lower curve. Notice what happened to the open-loop response of the entire circuit. The open-loop gain had been on a –1 (–20-dB/decade) slope until it reached the 354-Hz pole formed by R_O+R_1 and C_1. Then, the open-loop gain rolled off at a –2 (–40-dB/decade) slope until the gain dropped by an amount equal to $(R_O+R_1)/R_1$, or 7 dB. The rolloff then returned to a –1 slope and continued beyond where the gain fell below 1. Now that you see how the loop behaved for this circuit, you can proceed to the new circuit.

Lowering Z_O by a factor of 20

Figure 6a shows a version of the new circuit. Adding the single resistor, R_3, reduces the peak closed-loop output impedance, Z_O, by a factor of 20. **Fig-**

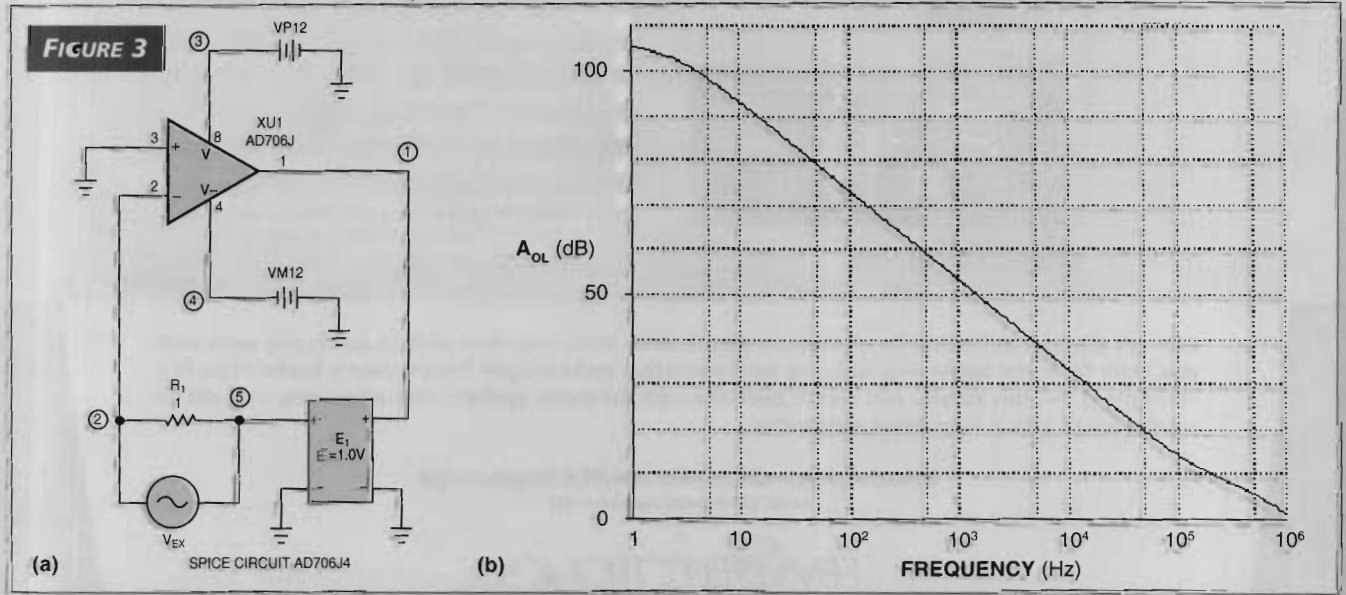
You can measure an op-amp's open-loop frequency response in a closed-loop configuration by inserting a floating excitation source, V_{EX}, in series with the loop (a). This technique reveals that the open-loop gain vs frequency is as well-behaved as you would hope (b).

FIGURE 4



This circuit has a closed-loop gain of 60 dB, determined by the 1-MΩ feedback resistor and the 1-kΩ resistor from the op-amp's inverting input to ground (a). The closed-loop output impedance of this circuit is low at low frequencies but rises to the open-loop value at higher frequencies, where loop gain is no longer available to reduce the output impedance (b).

FIGURE 3



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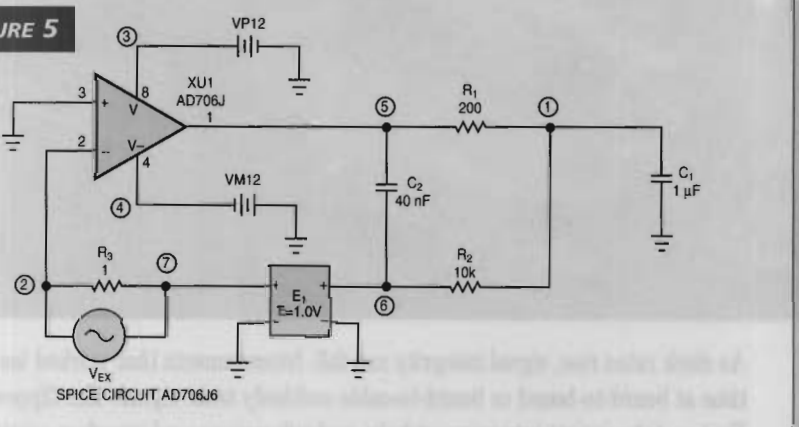
ure 6b is a plot of Z_O with two sets of values for C_1 and C_2. The plot of Z_O that peaks at approximately 12.5Ω is for C_1=2 μF and C_2=4 nF. The other plot is much better behaved and peaks at a little more than 10Ω. You may want to use C_1=4 μF, but the remaining simulations on this circuit are for C_1=2 μF. The ratio, $(R_2+R_3)/R_2$=20, determines the reduction in the closed-loop output impedance. Adding R_3 also alters the open-loop frequency response.

The output impedance decreased as planned. To test the transient response, I disconnected the current source from the output of the circuit in **Figure 6a** and added a pulse voltage source in series with the noninverting input. The transient response also looks good (**Figure 6c**). The 2-μF capacitive load, C_1, and the output-current limiting inside the AD706J limit the slew rate to 7.5 mV/μsec.

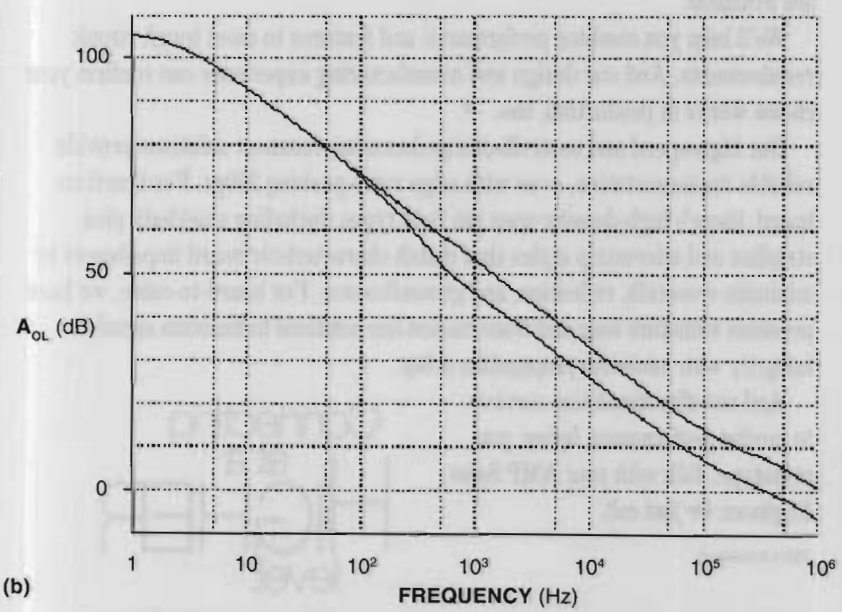
Figure 6d shows plots of the design of the open-loop-gain response of the circuits in **Figures 2a** and **6a**. The –1 slope that continues from approximately 5 Hz to above 500 kHz (the unity-gain-crossover frequency, f_6) is a typical op amp's worst-case open-loop response. In both circuits, R_O+R_1 and C_1 form a pole at f_1. In **Figure 2a**, R_1 and C_1 cause a zero at f_2. In **Figure 6a**, that same zero increases in frequency by a factor of 20 to f_3. Frequencies f_2 and f_3 need to occur below the point at which the loop gain crosses unity, frequency f_4. To design the circuit in **Figure 6a**, follow these steps:

1. Choose R_1 approximately equal to R_O. (Example: R_1=200Ω.)
2. Select the desired peak output impedance, Z_O. (Example: Z_O=10Ω.)
3. Calculate the factor by which R_1 must decrease, R_1/Z_O. (Example: 200/10=20.)
4. Choose $(R_2+R_3)/R_2$ to be the same factor calculated above, with R_2>> R_1. (Example: R_2=10 kΩ and R_3=190 kΩ.)

FIGURE 5



(a)



(b)

In simulation, this circuit exhibits an open-loop output resistance of 250Ω (a). If you measure this resistance on hardware, you will probably need to insert a capacitor between R_2 and ground to reduce the amplifier's output-offset voltage. The upper curve of (b) shows the AD706J response with no capacitive load. The lower curve shows the response of the circuit in (a).

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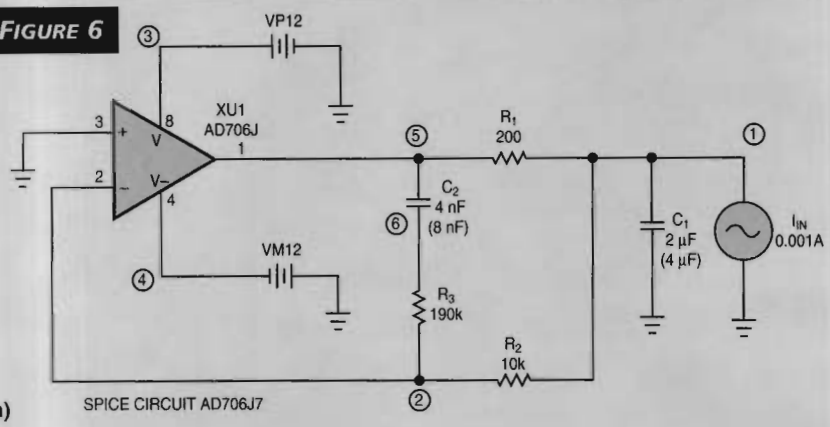
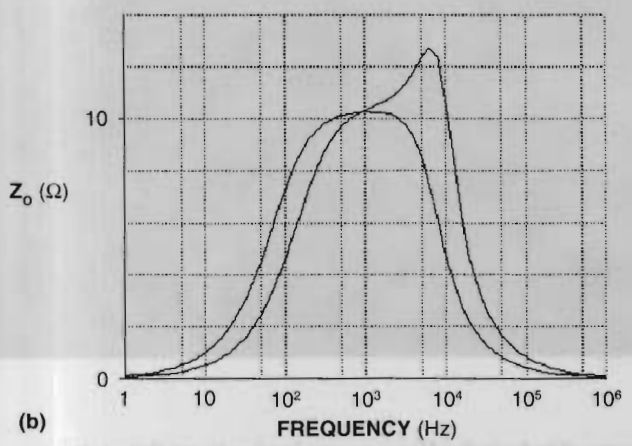
5. Calculate the ratio, $(R_1+R_O)/R_1$. (Example: (200+250)/(200=2.25.)
6. Determine the total attenuation. (Example: (20)(2.25)=45, which also equals 26 dB+7 dB=33 dB.)
7. Referring to **Figure 6d**, calculate the frequency, f_4, at which the op-amp open-loop gain is 33 dB. (Example: f_6/total attenua

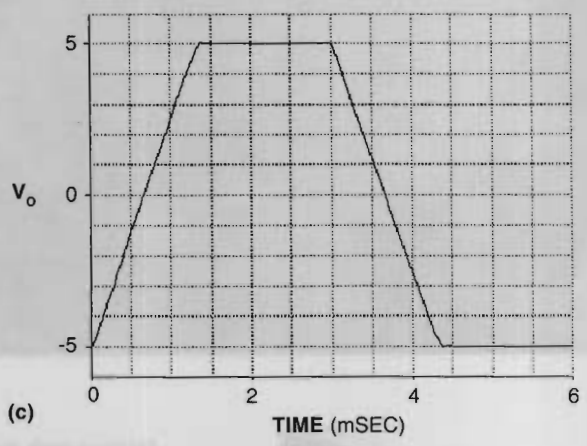
FIGURE 6



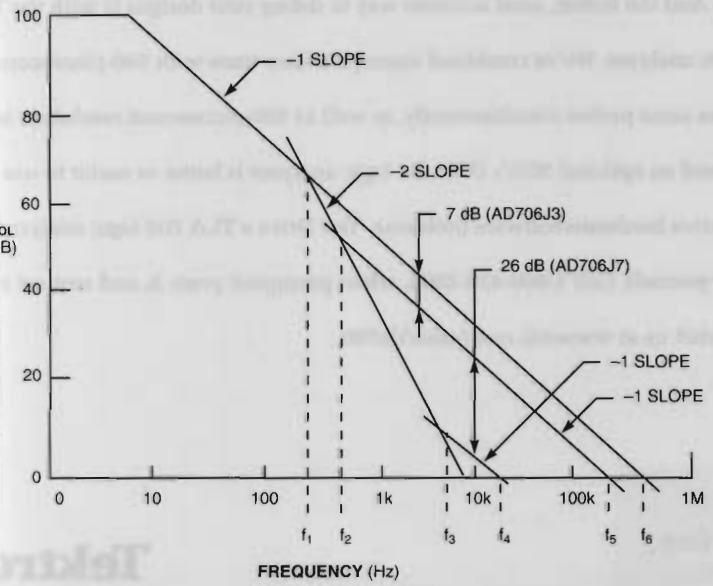
(a)



(b)



(c)



(d)

Adding one resistor, R_3, reduces the peak closed-loop output impedance, Z_O, by a factor of 20 (a). In (b), the plot of Z_O that peaks at approximately 12.5Ω is for C_1=2 µF and C_2=4 nF. The much better behaved plot is for C_1=4 µF. The circuit's transient behavior was very well behaved (c). The –1 slope that continues from about 5 Hz to above 500 kHz (the unity-gain-crossover frequency, f_6) in (d) is a typical op amp's worst-case open-loop response.

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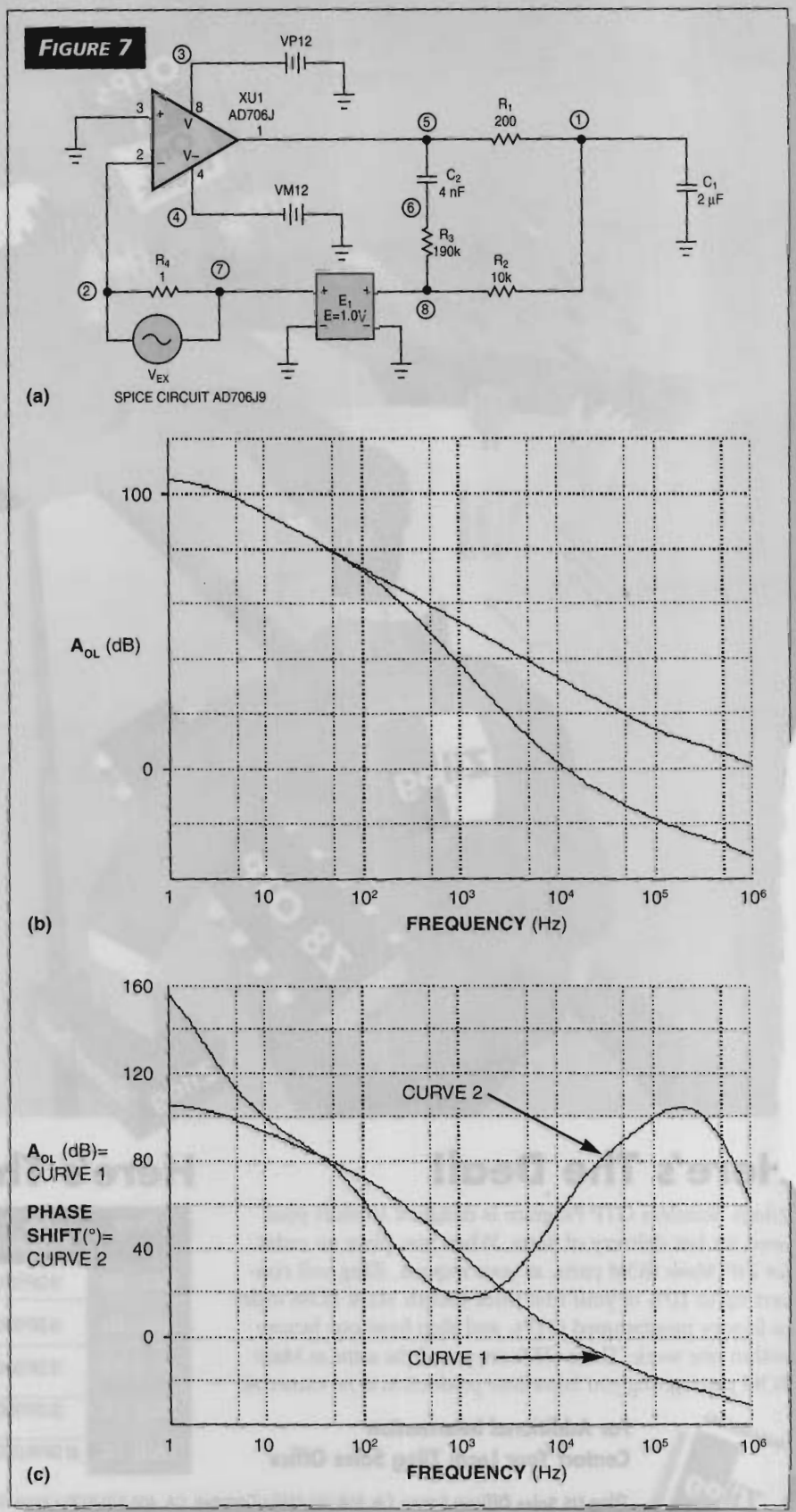
tion=500 kHz/45=11.11 kHz.)

8. Check **Figure 6d** to see that the open-loop gain has decreased by 33 dB at f_4.
9. Choose f_3 to be less than f_4. (Example: For C_1=2 µF, f_3= ($1/2\pi$ (R_1C_1) (R_1/Z_O)= 7.96 kHz, which is less than 11.11 kHz.)
10. Choose C_2. The circuit is stable as long as the zero formed by R_2+R_3 and C_2 is less than or equal to f_3. However, best Z_O performance occurs if the frequency of this zero is equal to or less than f_2, which is 398 Hz. (Example: C_2=4 nF and f=1/(2(R_2+R_3) C_2)= 199 Hz.)

Now, the design is complete. To verify the open-loop performance of the circuit in **Figure 6a**, **Figure 7a** adds the excitation source. **Figure 7b** is a plot of the open-loop gain response. The top curve is the AD706J response without a capacitive load; the bottom curve is the response of the circuit in **Figure 6(a)**. If you draw lines with –1 and –2 slopes tangent to the curves, you can see that the response is the same as that of the design in **Figure 6d**. **Figure 7c** is a plot of both gain and phase. You can see that the circuit has about 35 dB of gain margin at the point of highest phase shift (approximately 1.1 kHz) and about 60° of phase margin at the unity-gain (0-dB) crossover frequency (approximately 11 kHz).

You might need a constant output impedance from dc to megahertz. The circuit in **Figure 8a** is designed to have a 10Ω output impedance. Because feedback at dc comes from Node 7, R_2 determines the output impedance. At intermediate frequencies, C_4 connects Node 8 to Node 1 to make the circuit look like the circuit in **Figure 6a**, and (R_1+R_2)/(R_3+R_4/R_4) determines the out-

This circuit adds the excitation source, V_{EX} (a). In the plots of the open-loop gain response (b), the top curve is the AD706J response without a capacitive load; the bottom curve is the response of the circuit of (a). The circuit has about 35-dB of gain margin at the point of highest phase shift (approximately 1.1 kHz) and about 60° of phase margin at the unity-gain crossover frequency (approximately 11 kHz).



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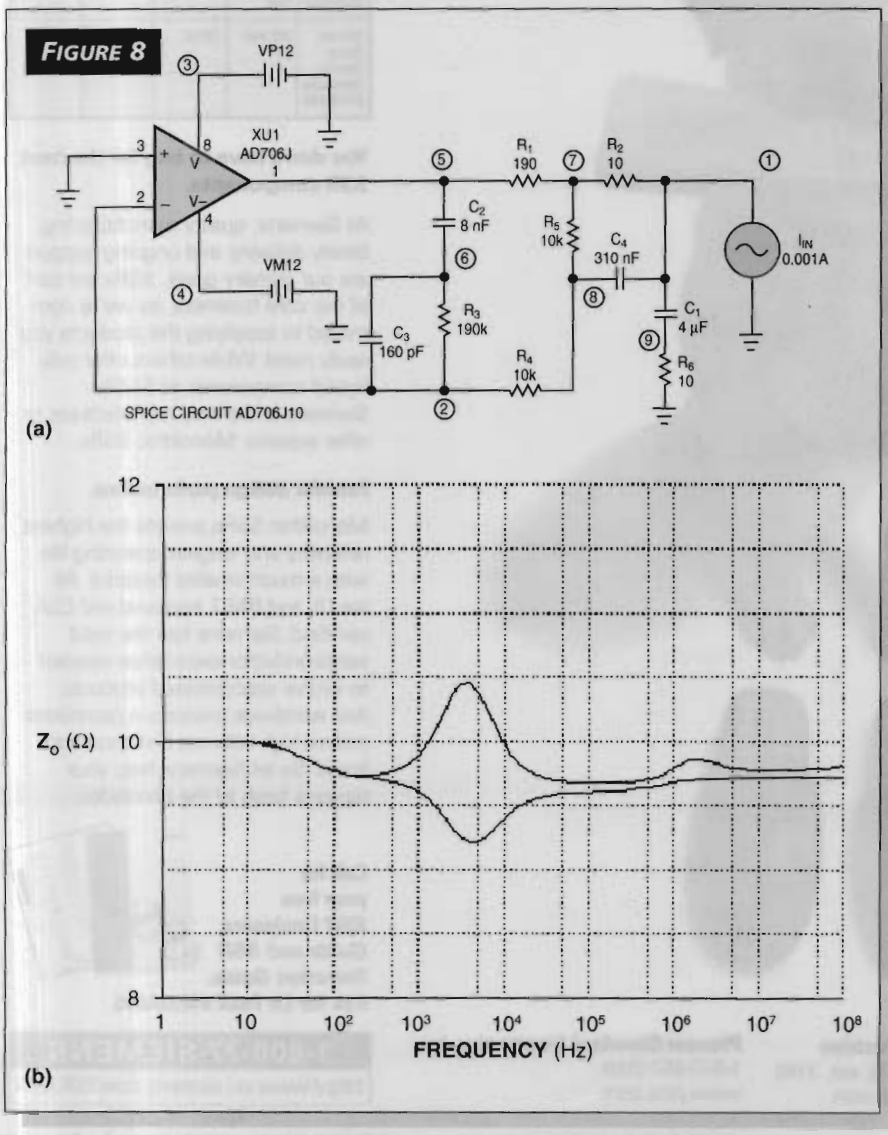
put impedance. Adding R_5 allows you to reduce the size of C_4. At high frequencies, R_6 dominates the output impedance; that is, R_6 is parallel with, but much lower than, R_O of op-amp XU1. C_3 bypasses R_3 at approximately the same frequency that the capacitive reactance of C_1 equals R_6. C_3 and C_4 were adjusted for the best performance. The top plot in **Figure 8b** is for the circuit of **Figure 8a**. In the bottom plot, a simulated best-case AD706J Spice model replaces the AD706J model. The impedance varies less than 1Ω over the entire frequency range.

The next circuit is what started this research. The SGS L2726 is a 1A-output, dual op-amp in an SOL-20 power package. Because Spice models were not available for this amplifier, I had to measure R_O using the technique discussed in the section, "Data sheets don't specify R_O." I measured R_O at three load currents. At 0 mA, R_O=13.8Ω; at 10 mA, R_O=3.3Ω; and at 200 mA, R_O=1.1Ω. I used a conservative value of 4.7Ω in the worst-case Spice model, L2726_sim. I took the gain information from the data sheet and assumed the gain to be 70 dB (3162) at dc, decreasing to unity at 600 kHz.

Figure 9a shows the simulated model. The circuit in **Figure 9b** uses this Spice model and was designed for a Z_O/30 impedance reduction. the circuit uses a single –5.2V supply to minimize power dissipation, and because a polarized output capacitor was used. But because general-purpose tantalum capacitors have a high ESR, I used a low-ESR (0.15Ω-maximum), 47-μF capacitor instead. Using the techniques previously discussed, I designed the circuit in **Figure 9b**. An extra capacitor, C_3, bypasses C_1 and R_4 at high frequencies. Spice simulations in **Figure 9c** show a maximum output impedance of 0.25Ω. Measurement on the actual hardware revealed a maximum output impedance of 0.2Ω from dc to 1 MHz.

You no longer need to avoid capacitive op-amp loads. Just examine the application and determine if capacitive loads are the best choice. You can feel confident in designing these loads into your products. These circuits have become very practical because 1-μF ceramic capacitors with an X7R dielectric characteristic are now available in the 3.2×1.6-mm (1206) chip. I no longer have to use op-amp buffers as frequently as I did in the past. EDN



This circuit is designed to have a 10Ω output impedance (a). The top plot of (b) is for the circuit in (a). In the bottom plot, a simulated best-case AD706J Spice model replaces the normal AD706J model. The impedance varies less than 1Ω over the entire frequency range.

Author's biography

Jimmie D Felps is an analog-design engineer for Hewlett Packard (Colorado Springs, CO). He holds six patents, including both electrical and mechanical designs.

FIGURE 9 ON PAGE 144

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